

What is Claimed is:

- 1 1. An output circuit, comprising:
 - 2 a damping control circuit branch, comprising a resistor and a diode connected in parallel between a first node and a second node, the second node being coupled to an output node;
 - 5 an output transistor coupled by its source and drain between a power supply and the second node, and having a gate; and
 - 7 a predriver circuit adapted to receive an input signal and provide a voltage at the gate.
- 1 2. An output circuit according to Claim 1, further comprising a tristate circuit adapted to cause the output node to be in a tristate condition in response to a tristate enable input signal.
- 1 3. An output circuit, comprising:
 - 2 an upper damping control circuit branch, comprising a first resistor and a first diode connected in parallel between a first node and a second node, the second node being coupled to an output node;
 - 5 a lower damping control circuit branch, comprising a second resistor and a second diode connected in parallel between a third node and the second node;
 - 8 an upper output transistor coupled by its source and drain between a power supply and the second node, and having a gate;
 - 10 a lower output transistor coupled by its source and drain between ground and the third node, and having a gate;
 - 12 an upper predriver circuit adapted to receive an input signal and provide a voltage at the gate of the upper output transistor; and
 - 14 a lower predriver circuit adapted to receive the input signal and provide a voltage at the gate of the lower output transistor.

- 1 4. An output circuit according to Claim 3, further comprising a tristate
- 2 circuit adapted to cause the output node to be in a tristate condition in
- 3 response to a tristate enable input signal.